UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,399	12/11/2003	Teruyuki Maeda	60437 (70820)	2109

21874 7590 10/14/2005

EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,399	MAEDA, TERUYUKI	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Rejections and/or objections as previously applied

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 2, 7, and 8 are rejected under 35 U.S.C. 102(a) as being anticipated by the applicant's admitted prior art (AAPA) of this application.

With respect to claims 1 and 8, AAPA teaches a power transistor composed of a plurality of vertical pnp transistors formed on a P-type silicon substrate 101, wherein (see figs. 3-5 and associated text of the specification of this application):

a singularity or plurality of electrode portions 118 of an N+ buried layer 102 formed to isolate the P-type silicon substrate and the plurality of vertical pnp transistors from each other are provided in an active region of the power transistor.

With respect to claim 2, AAPA further teaches at least part of the electrode portion is provided under common emitter metal lines 109 of the power transistor routed on the active region of the power transistor. See figs. 3-5 and associated text of the specification of this application.

With respect to claim 7, AAPA further teaches the singularity or plurality of electrode portions are placed so as to be uniformly spaced from their respectively adjacent electrode portions. See figs. 3-5 and associated text of the specification of this application.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 3, 4, 5, 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Williams et al. (US 5,648,281).

With respect to claims 1 and 8, AAPA teaches a power transistor composed of a plurality of vertical pnp transistors formed on a P-type silicon substrate 101, wherein (see figs. 3-5 and associated text of the specification of this application):

a singularity or plurality of electrode portions 118 of an N+ buried layer 102 formed to isolate the P-type silicon substrate and the plurality of vertical pnp transistors from each other are provided in an active region of the power transistor.

With respect to claims 3 and 6, AAPA further teaches that the electrode portions 118 are provided on the N+ buried layer 102, however, AAPA fails to teach an N+ type diffusion layer is formed connecting the electrode portion and the N+ buried layer 102.

Williams et al. teach an vertical pnp transistor in which a N+ diffusion layer 348 is formed connecting electrode portion and N+ buried layer. See figs. 28 and 28A and col.24, lines 1-60.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Williams et al. into the device of AAPA to reduce the collector resistance. See figs. 28 and 28A and col.24, lines 1-60.

With respect to claim 5, Williams et al. further teach that the diffusion layer 348 is more doped than the N epitaxial layer, but fail to teach the range for

the concentration of the diffusion layer 348. See figs. 28 and 28A and col.24, lines 1-60.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the concentration of the N+ diffusion layer through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 4, AAPA further teaches an N+ type base well layer 108 as a base region of the plurality of vertical pnp transistor. See figs. 3-5 and associated text of the specification of this application.

Further with respect to claim 4, the process limitation that the N+ type diffusion layer and the N+ type base well layer are formed at the same time is not given weight in the patentability determination of present device claims.

With respect to claim 2, AAPA further teaches at least part of the electrode portion is provided under common emitter metal lines 109 of the power transistor routed on the active region of the power transistor. See figs. 3-5 and associated text of the specification of this application.

With respect o

With respect to claim 7, AAPA further teaches the singularity or plurality of electrode portions are placed so as to be uniformly spaced from their respectively adjacent electrode portions. See figs. 3-5 and associated text of the specification of this application.

Rejections and/or objections necessitated by the amendments

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Williams et al. (US 5,648,281).

With respect to claim 9, AAPA teaches a power transistor comprising (see figs. 3-5 and associated text of the specification of this application):

a plurality of vertical pnp transistors formed on a P-type substrate, each pnp transistor having a P+ type collector 106, an N+type base well formed in a base region, a P+ type emitter layer 107 and an N+ type base layer;

an N+ type buried layer 102 isolating the P-type substrate from the P+type collector;

an N type epitaxial layer 104 formed over a surface of the P type substrate; and

an N+ type electrode layer 118.

AAPA further teaches that the electrode portions 118 are provided on the N+ buried layer 102, however, AAPA fails to teach an N+ type diffusion layer is formed connecting the electrode portion and the N+ buried layer 102.

Williams et al. teach an vertical pnp transistor in which a N+ diffusion layer 348 is formed connecting electrode portion and N+ buried layer. See figs. 28 and 28A and col.24, lines 1-60.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form a plurality of N+ type diffusion layers at electrode portions in an active region just under the N+ type electrode in the device of AAPA to reduce the collector resistance. See figs. 28 and 28A and col.24, lines 1-60.

Response to Arguments

6. Applicant's arguments filed 08/09/05 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments in the paragraphs on page 4 and 5 of the Amendment filed 08/09/05, it is submitted that AAPA teaches that a singularity or plurality of electrode portions 118 are provided in an active region of the power transistor and N+ type buried layer 102 is formed to isolate the P type silicon substrate 101 and the plurality of vertical pnp transistors from each other. See fig. 4 of this application as required by present claim 1.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP